



WORK OFFER

Ref. No. BE-2019-021UGE

Employer Information

Employer: Sigasi	Website: www.sigasi.com
Kerkstraat 108	Location of placement: Gentbrugge, Belgium
9050 Gentbrugge	Nearest airport: Brussels international airport
Belgium	Working hours per week: 40.0
	Working hours per day: 8.0

Number of employees: 9

Business or products: Software for hardware designer in the semiconductor industry

Student Required

General Discipline: 11-COMPUTER AND INFORMATION SCIENCES 14C-ELECTRICAL AND ELECTRONICS ENGINEERING	Completed years of study: 3
Field of Study: 11.0101-Computer and Information Sciences, General, 14.1001-Electrical and Electronics Engineering	Language required: English Excellent Or Dutch Good
Required Knowledge and Experiences: Java programming language	Other requirements: Student status obligatory: please include a Certificate of Enrolment with your nomination. If trainee has non-EEA/Swiss nationality: maximum duration is 90 days.

Work Offered

Sigasi Studio is an IDE for digital design in Verilog or VHDL. It provides the digital designer with all the facilities that are typically reserved for software developers such as syntax checking, navigation, project management, refactoring, autocompletion ...

One of the additional features that Sigasi Studio also provides is the generation of documentation to accompany your digital designs. Sigasi Studio analyses the structure of VHDL- and Verilog-projects and generates documentation for all the components found based on the properties of all the components found in the projects and also based on the comment sections accompanying those components in the Verilog/VHDL source.

Currently, Sigasi Studio creates documentation through the use of DocBook. The end result is PDF. We are running into the limitations of this approach. In particular, we're finding it hard to generate documentation with a decent layout using this approach.

For this internship, we would like you to replace this DocBook flow with a flow that generates HTML. We believe that generating HTML will benefit the users of Sigasi Studio because the documentation can be laid out more elegantly, will be easy to navigate and can eventually embed sections holding graphs, equations, animations ...

Your task will be to architect (together with the team) and implement the flow to go from our internal representation of a VHDL/Verilog project through any intermediate representations (XML, markdown ...) to the final HTML and CSS.

Number of weeks offered: 12 - 24	Working environment: Research and development
Within the months: 15-JAN-2019 - 15-DEC-2019	Gross pay: 240 EUR / Week
Or within: -	Deduction to be expected: 0
Holidays: -	Payment method / frequency: Bank transfer / Weekly

Accommodation

Canteen at work: No	
Expected type of accommodation: Student dormitory	Estimated cost of lodging: 100 EUR / Week
Accommodation will be arranged by: IAESTE	Estimated cost of living incl. lodging: 200 EUR / Week

Additional Information

Nomination Information

Deadline for nomination: 31-MAR-2019	Please send nominations by Exchange Platform
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Date: 15-JAN-2019	On behalf of receiving country: Annelies Vermeir
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